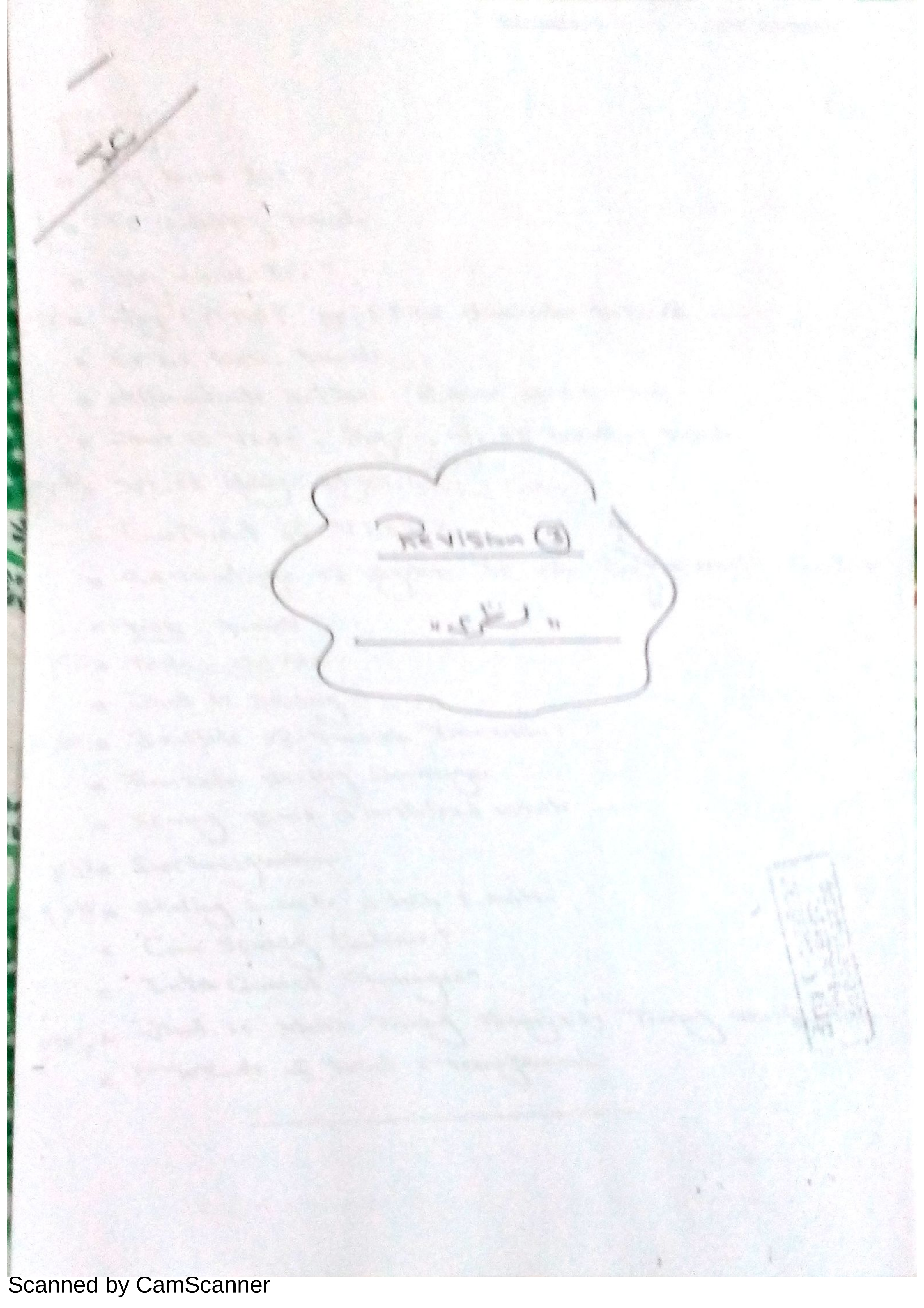

Revision
"نظري"

**Lec (1)** :-

* Why build ICs?
* IC industry trends
* Why make ICs?
* Why CMOS? or CMOS dominates because ----
* CMOS tech. trends.
* differentiate between Bipolar and CMOS.
* What is VLSI, Why? , VLSI industry trends.
* VLSI design styles. → SoC, → Full Custom
* Component of VLSI?
* Advantage of digital IC over the discrete Component
* tech. trends
* Tech. drivers.
* What is Scaling?
* Benifits of Smaller Transistor?
* Transistor Scaling Challenges
* Scaling gives 3 important results ---
* Electromigration
* Scaling Limits & tech Limits.
* Can Scaling Continue?
* Interconnect Challenges?
* What is static Timing Analysis? Timing verification
* Methods of Heat Management.

(Extra)

X = Testing of VLSI : is to ensure defect-free Products, it being done in:

(1) during design (2) during Fabrication

(3) After Fabrication.

Imp = Why Low Power techniques?

(1) increase battery life time.

(2) To enhance noise margin

(3) To increase system reliability.

X = Power dissipations:

(1) Static Power dissipation: Caused by the Leakage Current in the absence of any switching state

$$P_{static} = I_D V_{DD}$$

(2) dynamic Power dissipation

Caused by switching transistor

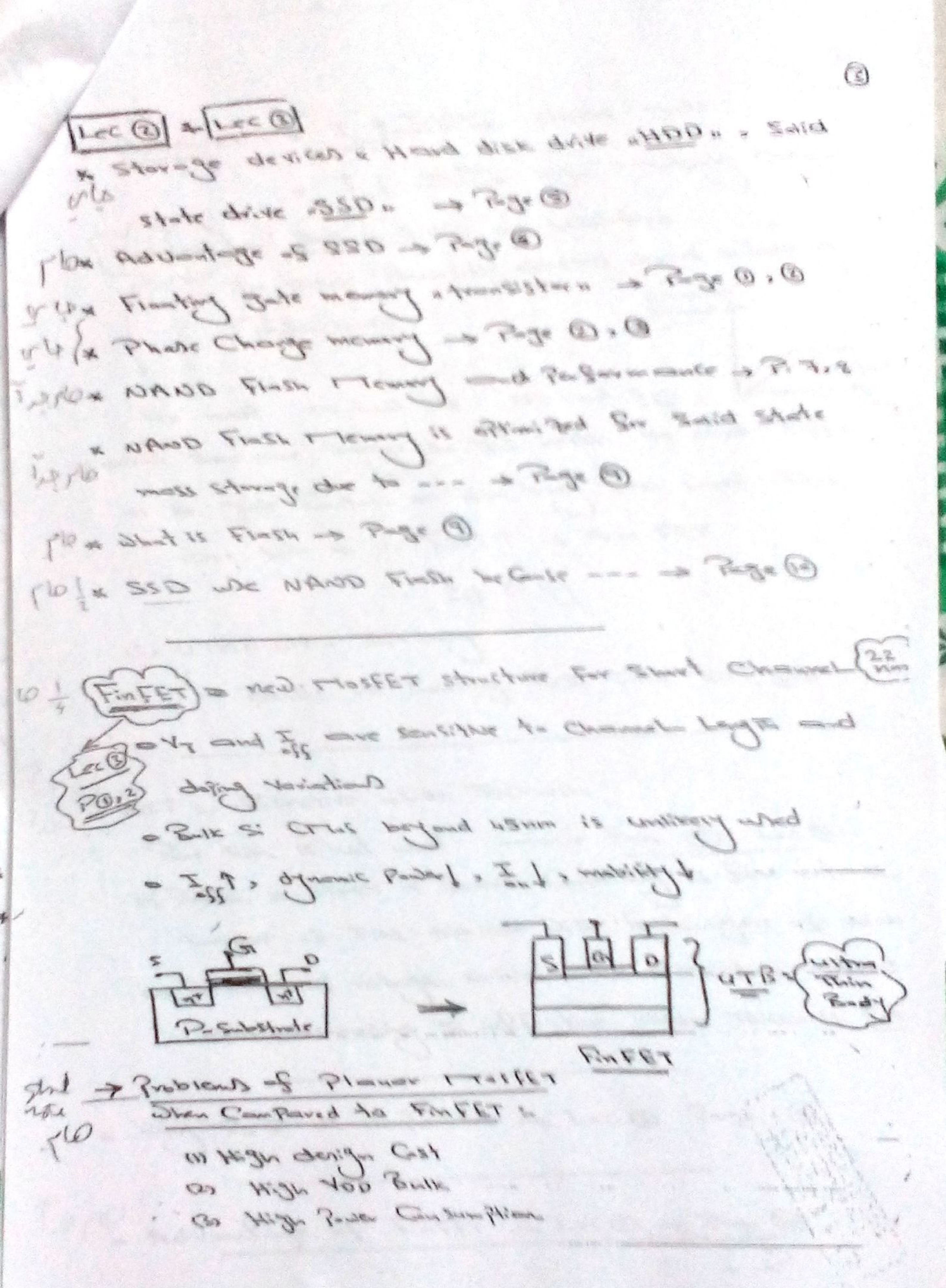
$$P_{dynamic} = C_L f V_{DD}^2$$

$$\therefore \text{Total Power} = I_D V_{DD} + C_L f V_{DD}^2$$

Imp = Low Power design:

(1) Reduce static Power : Low $V_{Th}$, I(Leakage)↓

(2) Reduce dynamic Power : Reduce VDD , Reduce $C_L$



**Lec (2) & Lec (3)**

* Storage devices « Hard disk drive «HDD» » Solid state drive «SSD» → Page (3)
* Advantage of SSD → Page (4)
* Floating gate memory «transistor» → Page (1), (2)
* Phase Change memory → Page (2), (3)
* NAND Flash Memory and Performance → P. 7, 8
* NAND Flash Memory is optimized for solid state mass storage due to --- → Page (9)
* What is Flash → Page (9)
* SSD use NAND Flash because --- → Page (10)

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**FinFET** = new MOSFET structure for short channel (22 nm)

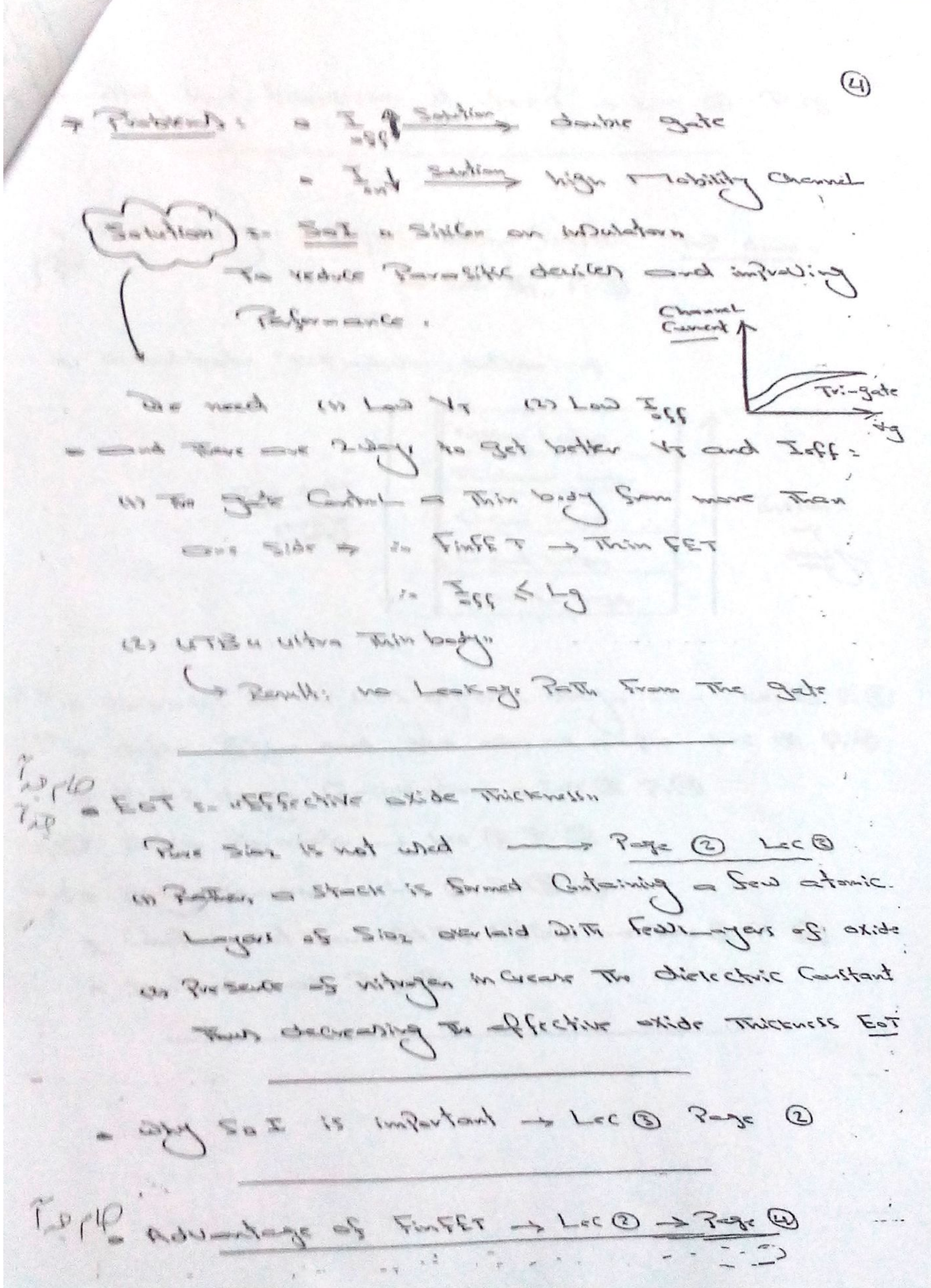
Lec (3) P(1,2)

- $V_T$ and $I_{off}$ are sensitive to channel length and doping variations
- Bulk Si CMOS beyond 45nm is unlikely used
- $I_{off}\uparrow$, dynamic power $\downarrow$, $I_{on}\downarrow$, mobility $\downarrow$



→ Problems of Planar MOSFET when compared to FinFET:

(1) High design cost
(2) High VDD bulk
(3) High power consumption





* Problems: – $I_{off}\uparrow$ —Solution→ double gate
– $I_{on}\downarrow$ —Solution→ high mobility channel

(Solution) :- SOI = Silicon on Insulator
To reduce Parasitic devices and improving Performance.



We need (1) Low $V_T$ (2) Low $I_{off}$
– and There are 2 ways to get better $V_T$ and Ioff:
(1) The gate Control a Thin body from more Than one side ⇒ i- FinFET → Thin FET
ii- $I_{off} \leq L_g$
(2) UTB "Ultra Thin body"
↳ Result: no Leakage Path from The gate

---

هام جدا
– EOT :- "Effective oxide Thickness"
Pure SiO2 is not used ——→ Page (2) Lec (3)
(1) Rather, a stack is formed Containing a few atomic Layers of SiO2 overlaid with few layers of oxide
(2) Presence of nitrogen increase The dielectric Constant Thus decreasing The effective oxide Thickness EOT

---

– why SOI is important → Lec (3) Page (2)

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هام جدا – Advantage of FinFET → Lec (2) → Page (4)

* Why new transistor structure? → Lec ⑤ P.③

---

* VLSI design & digital design Process. Top down &
  ↳ Lec ② P.⑤

* To illustrate Top-down, bottom-up.

| Top-down design ↓ |
| --- |
| System Layer |
| Functional Layer |
| Circuit Layer |
| Layout Layer |
| Physical Layer |
| ↑ Bottom up design |

* Abstract of VLSI digital design --- Lec ② P.⑥
* define RTL and give an example Lec ② P.⑥
* VLSI design Consideration → Lec ② P.⑦
* Design Parameter → Lec ② P.⑦
* Design domain → Lec ② P.⑧,⑨
* Compare between ASIC, FPGA → Lec ② P.⑩
* Short notes at Page ⑪

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**Lec (4)**

* define PLA? Page (2)
* Explain Programmable Logic techniques Page (2)
* Types of PAL ----- Page (3)
* Conflict between GAL, PAL, Page (3)
* PROM Vs PLA Page (3)
* Why field Programmable Page (5)
* PAL is faster than PLA ---- Page (5)
* Why PLA → Page (5)
* GAL is better than PLA ---- Page (4)
* disadvantages of SOP Page (4)
* PLD adv and disadv Page (4)

---

**Lec (5)**

* What are FPGA? P. (1)
* FPGA contains hundred thousand of F-F ... latches P (1)
* FPGA offer --- P (1)
* Structure → P (2)
* FPGA properties → P. (3), (4)
* FPGA has advantage in comparison with ASIC -- --- Page (4)
* FPGA, CPLD → Page (5)
* HDL design flow for FPGA → Page (5)
* " " " " " using Mentor graphic → P.1

* CLB Contains --- P. 7
* Slice Structure -- P. 8
* Basic structure of LUT P. 8
* How to speed up CLB P. 9
* describe Spartan 3E and how to improve its Performance → P. 10
* CLB in Spartan 3E Contain -- P 11
* Virtex 5 Vs Virtex 4 → P. 11
* Spartan 3E Vs Virtex 5 → P. 13
* FPGA design Flow in Xilinx → P 13, 14.
* describe ISE → P. 15
* FPGA advantage --- P. 15

---

Lec 6 :-

* Programming techniques (Short notes) P 1
* Explain digital switch. State its Limitation. Suggest a Modification.
  - Page 5, 6, 7, 8, 9
* TG are better Than Pass Transistor in --- P 10
* TG Features P. 10

---

Lec 9

* define DR, Purpose of DR, Contents of DRs, and advantage of DRs
  - Page 3, 4, 6

Lec (12) — Page 1, 2, 3, 4 → «احفظ»

* Compare between Passive Load, EMD → P. (8)
* Compare between EMD, DMD → Page (8)
* CMOS Properties → Page (9)
* Steady state Condition ---- P. (9)
* noise Margin, noise immunity, its Types → P. (10)
* To balance NM --- P. (11)

$\beta_n = \beta_p$

(note That)

= Changing beta ratio (Size) $V_{IL}$, $V_{IH}$ P. (11)

---

* The Factors Which will affect rise Time and Fall time → CMOS يعني $t_f$, $t_r$ كلامه عليهم
* To Make $t_r = t_f$

↳ $W_p = 2W_n$ or 2.5

---

(2) * CMos disadvantages:

(1) For N input CMos gate, 2N trans. required. ↳ Large Si area
(2) Large Fan in gates
(3) Large delay
(5) Large Parasitic Capacitance

## Pseudo NMOS Vs Complementary CMOS

| Pseudo (Ratioed Logic) (ECVD, DTMP, Pseudo) | CMOS (ratioless) |
| --- | --- |
| • Smaller no. of trans (N+1) for N i/ps → Less area → Less Capacitive Loading to Preceding Gate | • 2N transistor needed for N i/p. |
| • Ratioed | • Ratioless |
| • $t_{HL} \neq t_{LH}$ | • $t_{HL} = t_{LH}$ |
| • no Static Power dissip. | • higher static Power dissip. |
| • Full swing | • Smaller NM & reduced swing |

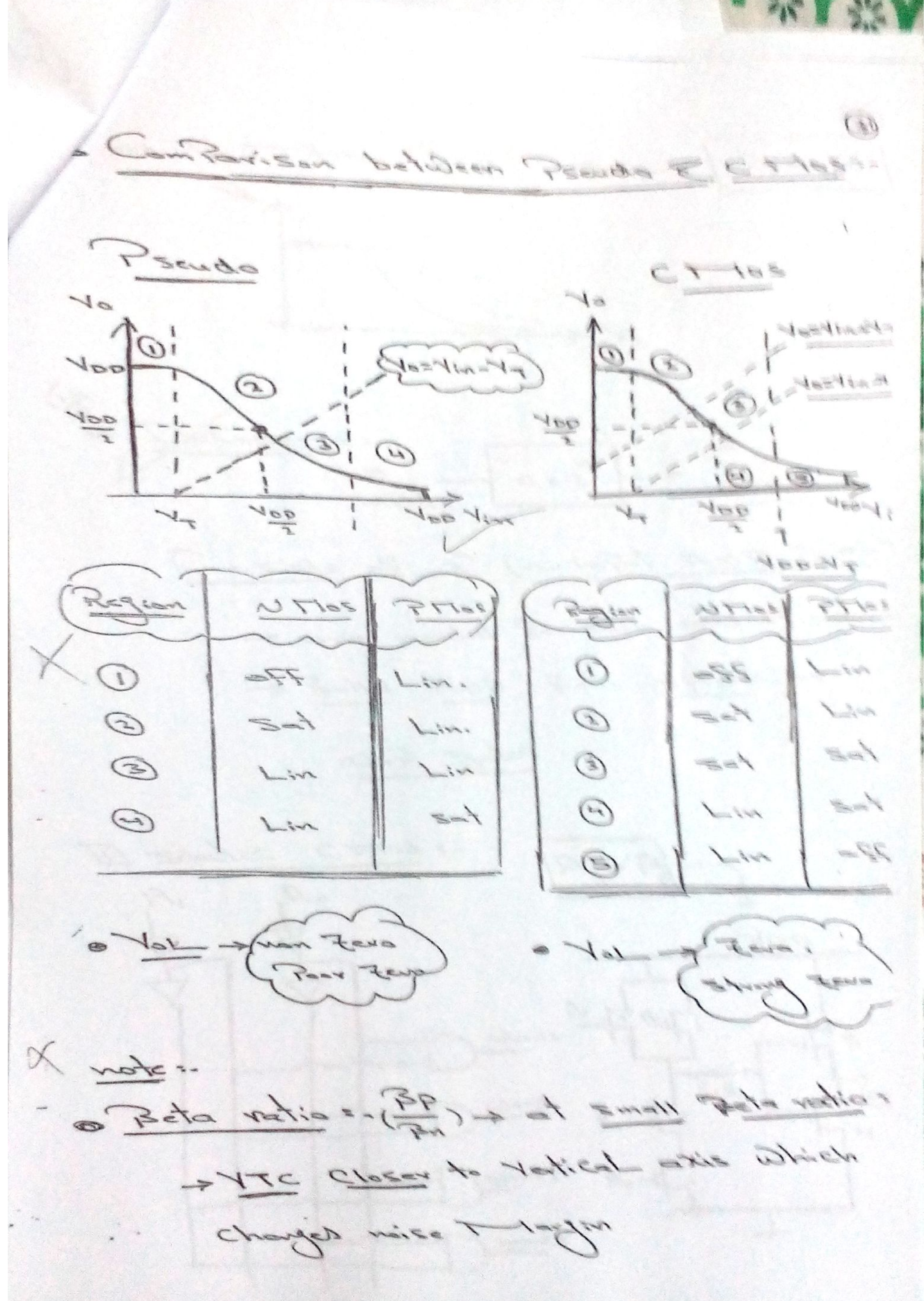
* DCVSL advantage over Pseudo
  → $V_{OL}$ & $V_{OL}$ of Pseudo $\neq 0$
  → Static power dissipation

* Pseudo Vs CMOS
  ① Smaller no. of transistor
  → Less area
  → Less Capacitive Loading to gate

  ② Power Consumption due to DC Current

$$P_{av} = V_{DD} I_{avg} = \frac{k_p}{2} [V_{DD}] [V_{DD} - V_T]^2$$

∴ Low NM



## Comparison between Pseudo & CMOS:-

### Pseudo



| Region | NMOS | PMOS |
| --- | --- | --- |
| 1 | off | Lin. |
| 2 | Sat | Lin. |
| 3 | Lin | Lin |
| 4 | Lin | sat |

- $V_{OL}$ → non zero, Poor zero

### CMOS

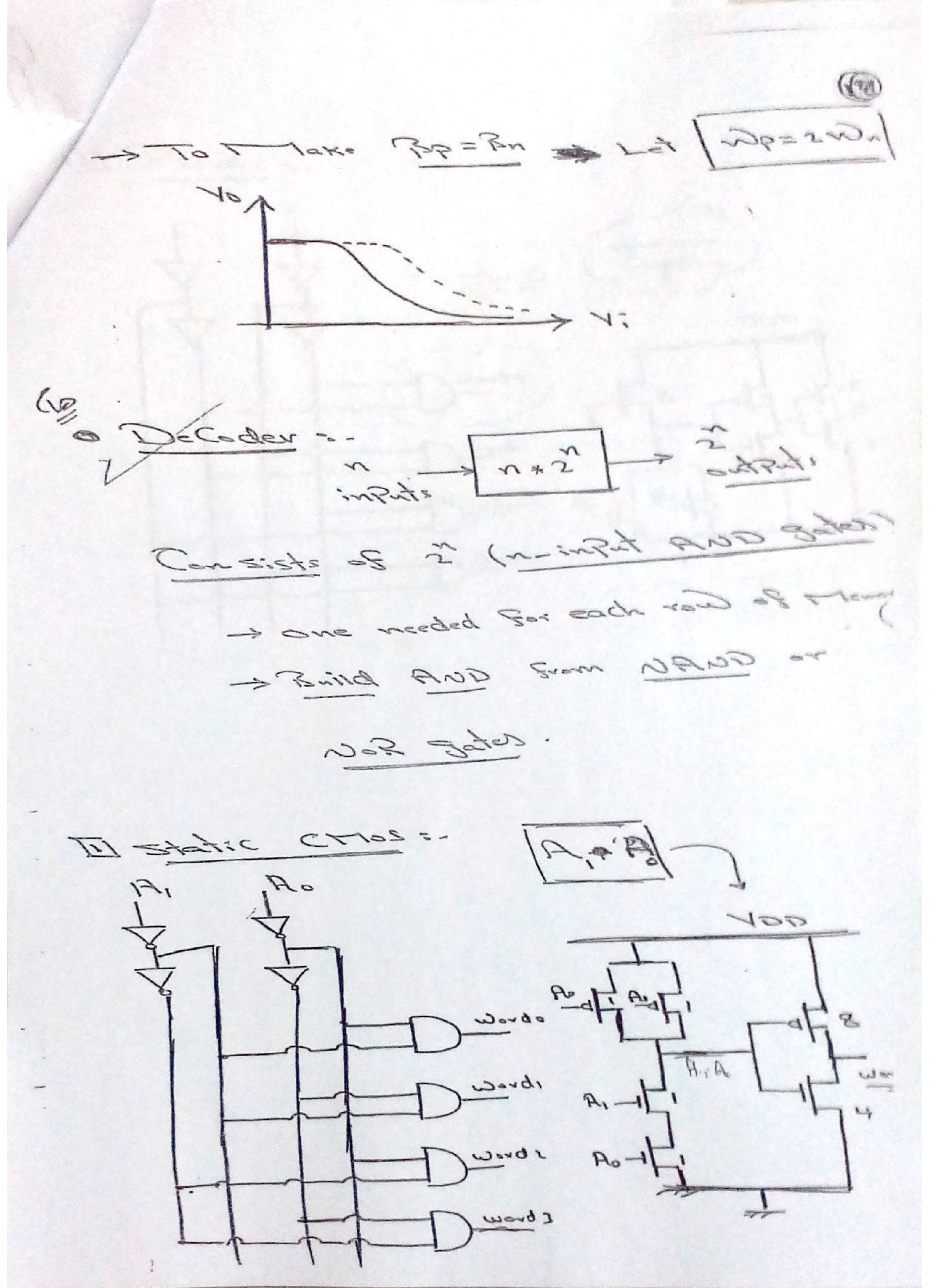


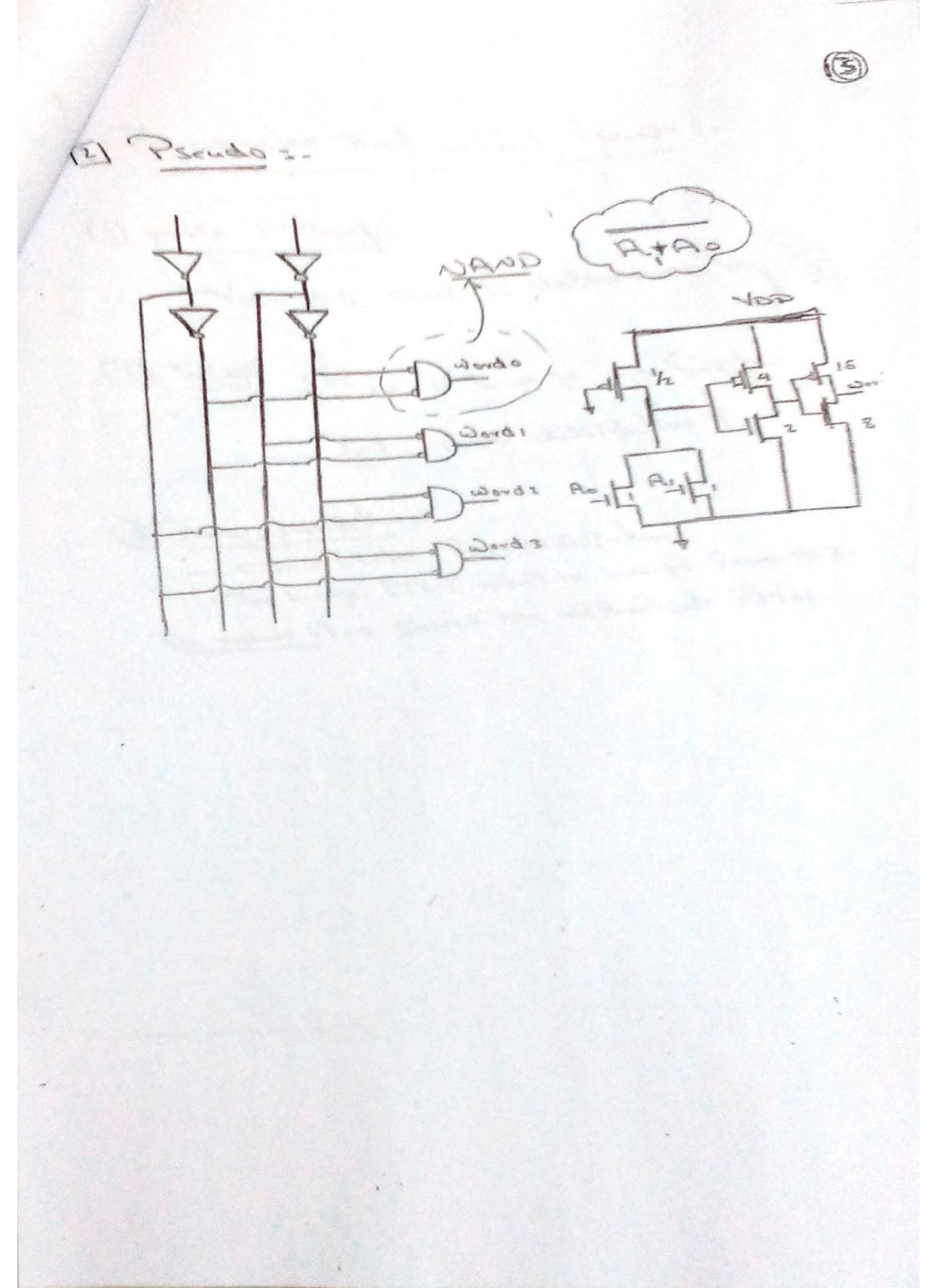
| Region | NMOS | PMOS |
| --- | --- | --- |
| 1 | off | Lin |
| 2 | Sat | Lin |
| 3 | Sat | Sat |
| 4 | Lin | Sat |
| 5 | Lin | off |

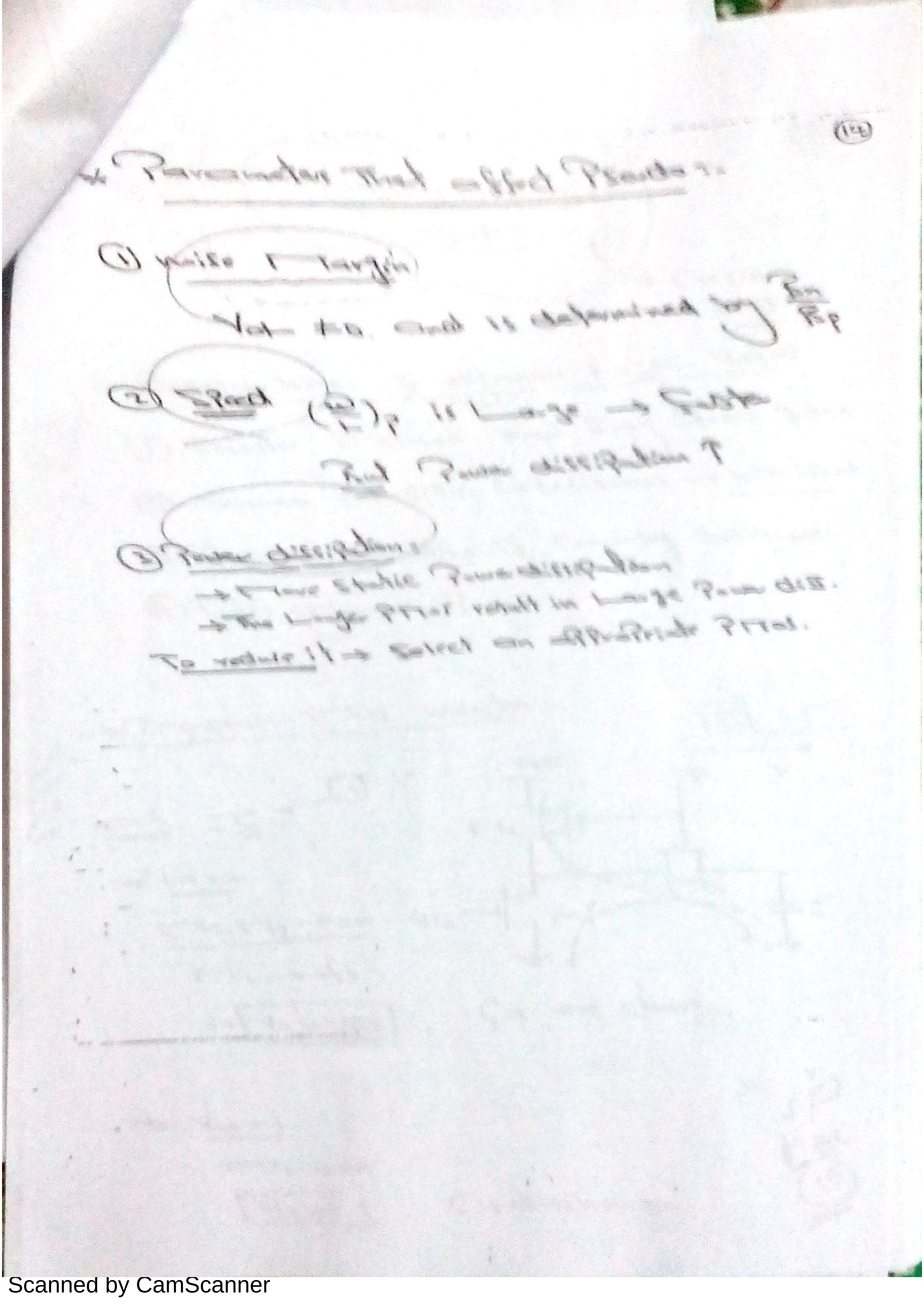
- $V_{OL}$ → Zero, Strong Zero

**note:-**

- Beta ratio :- $\left(\frac{\beta p}{\beta n}\right)$ → at small Beta ratio: → VTC Closer to vertical axis which changes noise Margin


(97)
→ To Make βp = βn ⟹ Let Wp = 2Wn
Vo
Vi
(10) Decoder :-
n inputs
n * 2^n
2^n output.
Consists of 2^n (n-input AND gates)
→ one needed for each row of Memory
→ Build AND from NAND or NOR gates.
[1] Static CMOS :-
A1 · A0
A1
A0
VDD
word0
word1
word2
word3
A0
A1
A1+A0
8
4
1
wor


3
2 Pseudo :-
NAND
$\overline{A_1 + A_0}$
VDD
word0
word1
word2
word3
1/2
4
16
2
8
A0
A1
1
1





## * Parameters that affect Pseudo :-

① **Noise Margin**

$V_{OL} \neq 0$, and is determined by $\frac{R_n}{R_p}$

② **Speed**  $\left(\frac{W}{L}\right)_P$ is Large → faster

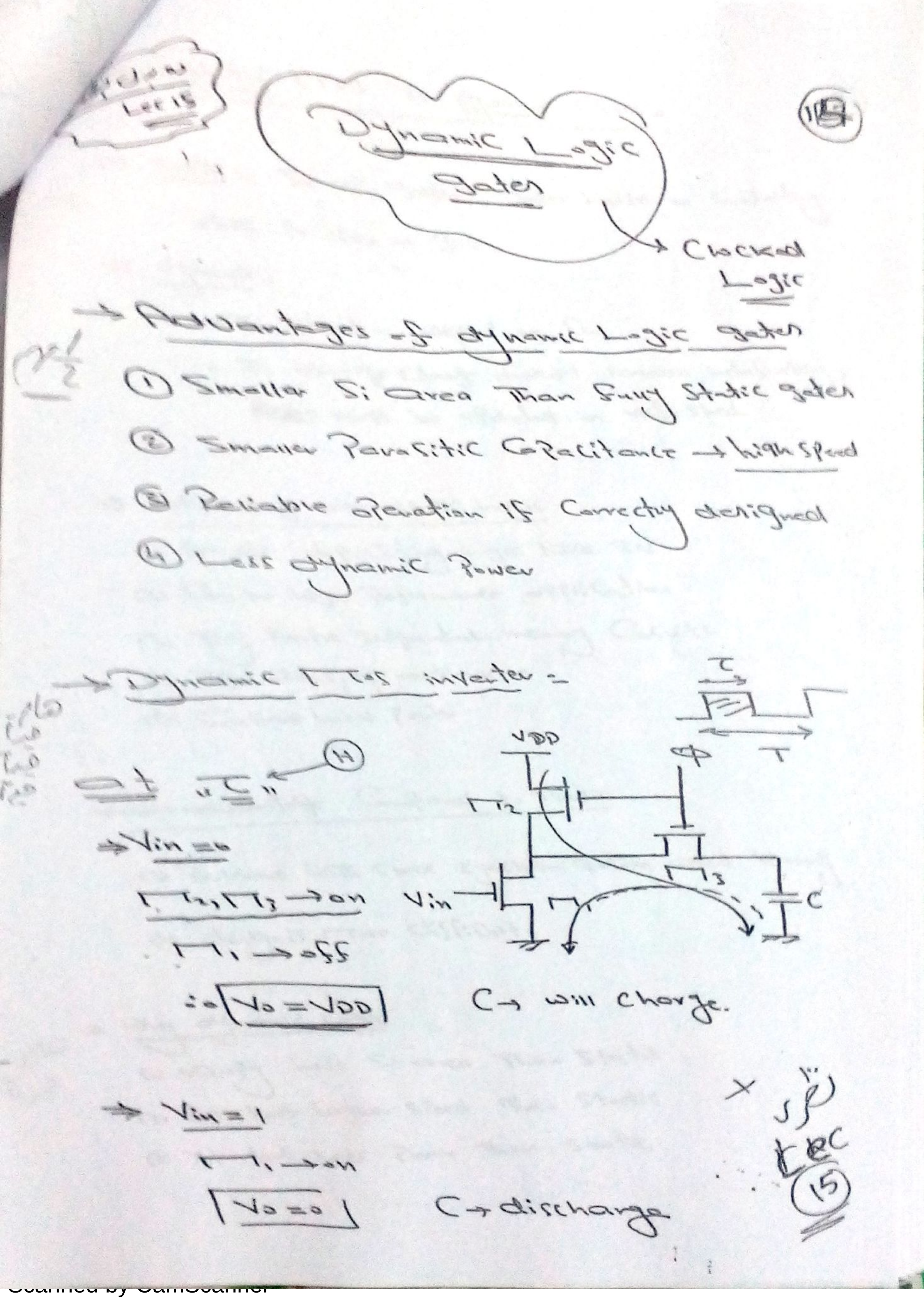
but Power dissipation ↑

③ **Power dissipation :**

→ Have Static Power dissipation

→ The Larger PMOS result in Large Power diss.

To reduce it → Select an appropriate PMOS.



# Dynamic Logic Gates → Clocked Logic

→ **Advantages of dynamic Logic gates**

1. Smaller Si area than fully static gates
2. Smaller Parasitic Capacitance → high speed
3. Reliable operation if correctly designed
4. Less dynamic Power

→ **Dynamic NMOS inverter:**



at "τ" ← (H)

→ $V_{in} = 0$

$M_2, M_3 \rightarrow$ on

$M_1 \rightarrow$ off

$\therefore \boxed{V_o = V_{DD}}$  C → will charge.

→ $V_{in} = 1$

$M_1 \rightarrow$ on

$\boxed{V_o = 0}$  C → discharge

Lec 15

# "Static CMOS Vs dynamic CMOS"

(1) Static :- The o/p gates have a conducting Path to VDD or GND.

(2) dynamic :

- The operation depend on CL
- The Storage Charge doesn't remain indefinitely, [redacted]s must be updated or refreshed.

## Advantage over static Logic

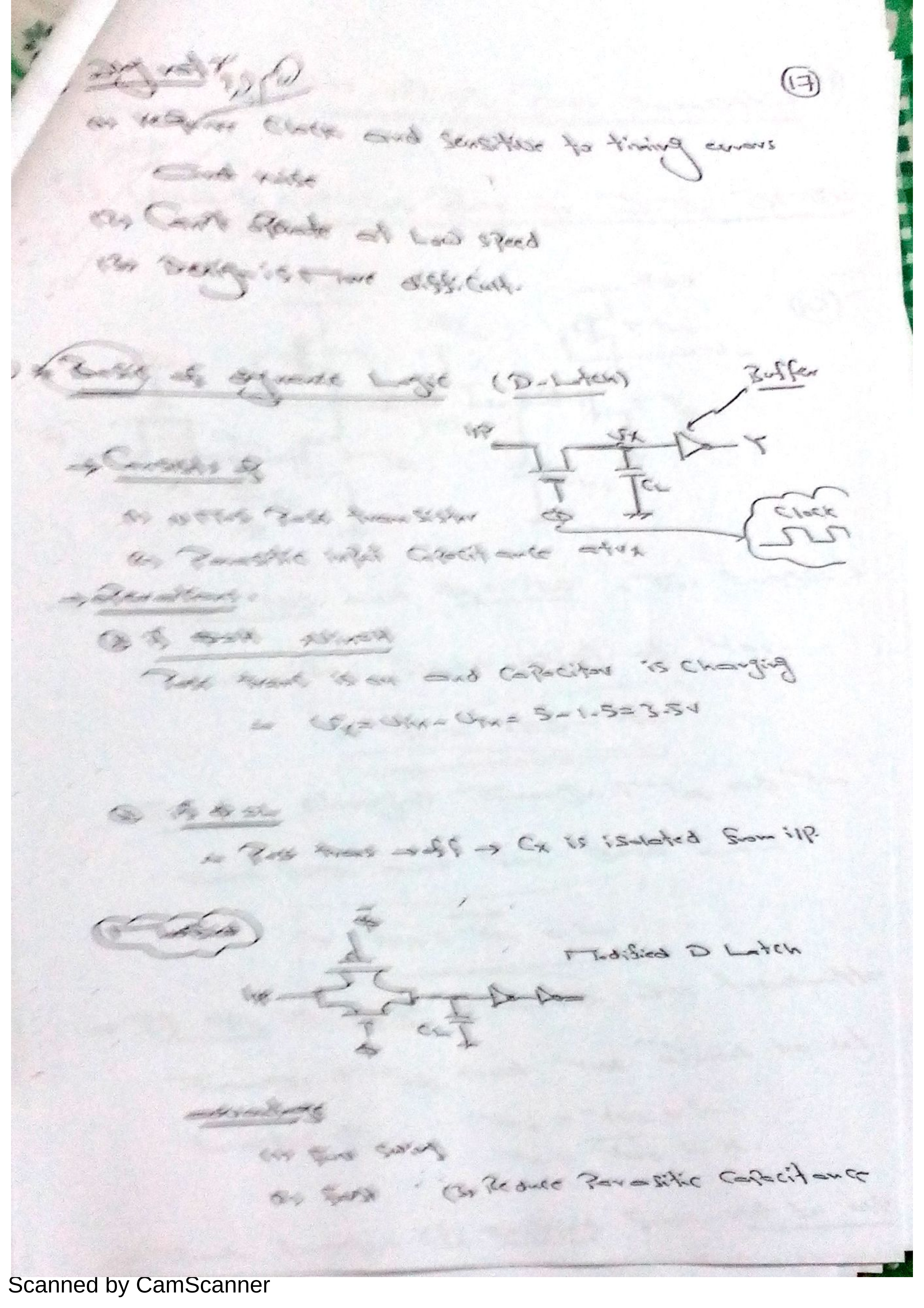
(1) Avoids duplicating Logic twice 2N
(2) Can be high performance application
(3) Very simple sequential memory Circuits
(4) High density achievable
(5) Consume Less Power

## disadvantage Compared to static

(1) Problems with Clock synchronization and timing
(2) design is more difficult.

## Why dynamic Logic

(1) occupy less Si area than static
(2) It has higher speed than static
(3) It has less Power than static



(1) Requires Clock and sensitive to timing errors
Clock rate
(2) Can't operate at low speed
(3) Design is more difficult.

## Basics of Dynamic Logic (D-Latch)



→ Consists of
(1) NMOS Pass transistor
(2) Parasitic input capacitance at x

→ Operations:
(1) If Φ = 1
Pass trans is on and capacitor is charging
∴ $V_x = V_{in} - V_{TN} = 5 - 1.5 = 3.5V$

(2) If Φ = 0
∴ Pass trans → off → $C_x$ is isolated from i/p.

Modified D Latch



Advantages
(3) Reduce Parasitic Capacitance

# Shift register using Pass transistor :- (18)

## 1 Using NMOS Pass tr. with DMD:

(10)



→ If $V_1 = V_{DD}$ and $\phi_1 = V_{DD}$, The Logic "1" $= V_{DD} - V_{Tn}$ would exist at $V_{o1}$.

$$\therefore V_{o1} = V_{DD} - V_{Tn}$$

- The $C_{L1}$ charges Through $M_{N1}$ as $V_{o1}$ goes high and $V_{o2}$ goes Low.

$$\therefore V_{o2} = \overline{V_{o1}} = L.$$

→ If $\phi_2$ is High. Low will transmitted Through $M_{N2}$ and $V_{OH}$ would be at Logic ①.

$$V_{o3} = V_{o2} = L$$
$$V_o = \overline{V_{o3}} = H.$$

→ Thus Logic ① shifted from i/p to o/p

## CMOS dynamic shift register using TG

VDD
$\phi_1$
$V_i$
$\bar{\phi}_1$
$\phi_1$
$\phi_2$
$V_o$

* operation

① $V_i = VDD$, $\phi_1 = VDD$

$\therefore V_{o1} = VDD$, $V_{o2} = 0$ as $V_{o2} = \bar{V}_{o1}$

② $\phi_2$ goes high, Then $V_{o3}$ switches to zero

Then $V_o = VDD$

Thus i/p signal is shifted to the o/p during one Clock

---

## * Dynamic CMOS gate operation

* Definition

① $\phi = Low$

$M_P \rightarrow on$

$M_n \rightarrow off$

$C_L$ will charge toward VDD.

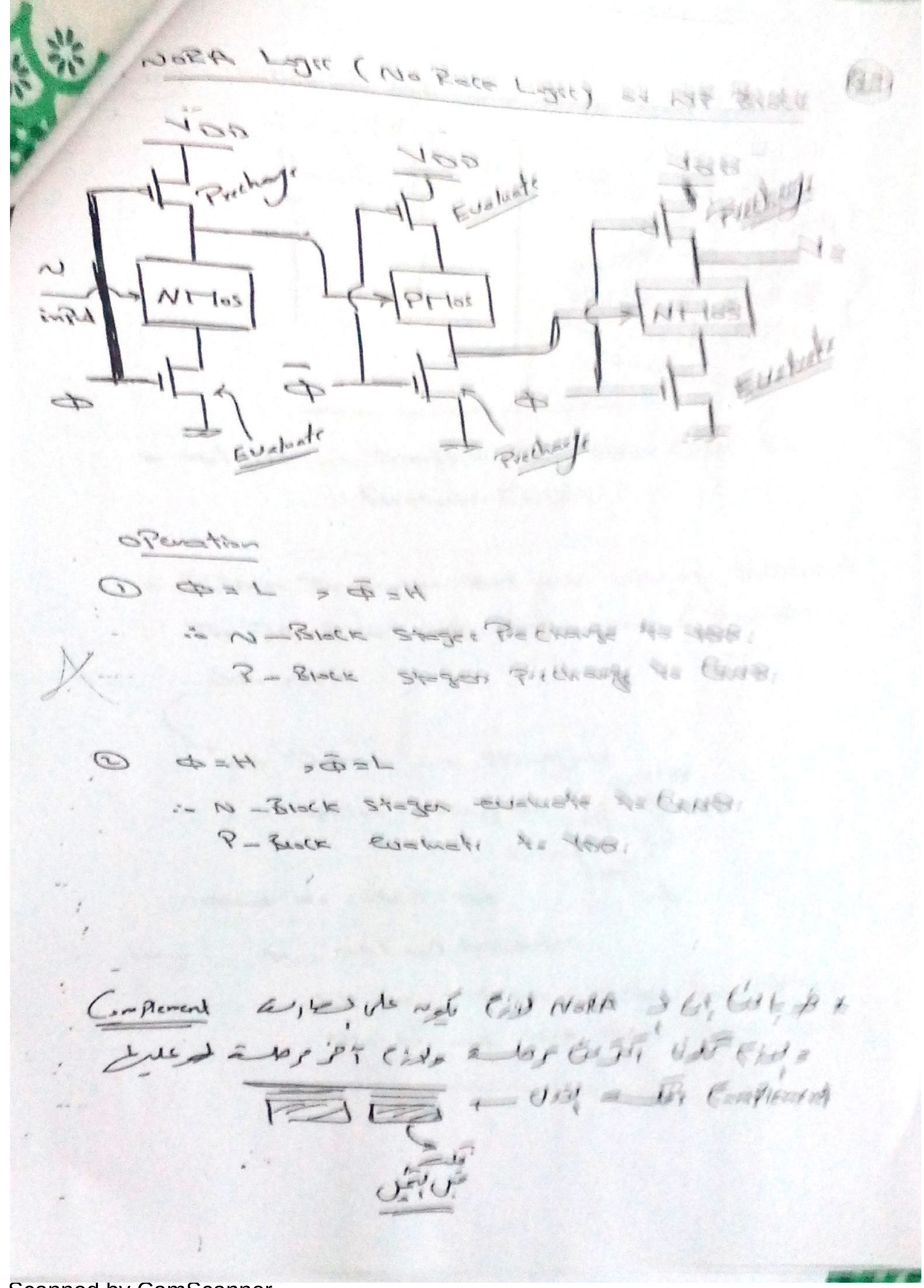
(Precharge)

VDD
$C_L$
Clk
Evaluate
Precharge

② $\phi = High$

$M_P \rightarrow off$, $M_n \rightarrow on$

$\therefore C_L$ will discharge toward GND (Evaluate)


NORA Logic (No Race Logic)
VDD
Precharge
Evaluate
input
N Mos
P Mos
Φ
Φ̄
Operation
① Φ = L , Φ̄ = H
∴ N-Block stage: Precharge to VDD.
P-Block stages Precharge to GND.
② Φ = H , Φ̄ = L
∴ N-Block stages evaluate to GND.
P-Block evaluate to VDD.
NORA
Complement

(extra) - implement XOR gate using 4 i/p LUT.

[illegible]

| A | B | C | D | o/p |
|---|---|---|---|---|
| 0 | 1 | 1 | | 1 |
| 0 | | | | |
| \| | \| | \| | | |

صفحة
16 طارق
[illegible]
[illegible]

---

- net list → Translate from VHDL Code to Electronic Circuit

- Explain the reason that one always implement the Pull up net with PMOS and Pull down with NMOS

↳ as PMOS → Strong one
NMOS → Strong Zero

VDD

$V_i$

and we want this

→ act as inverter

$V_i = 0 \rightarrow V_o = VDD$ from PMOS

$V_i = 1 \rightarrow V_o = GND$ from NMOS

---

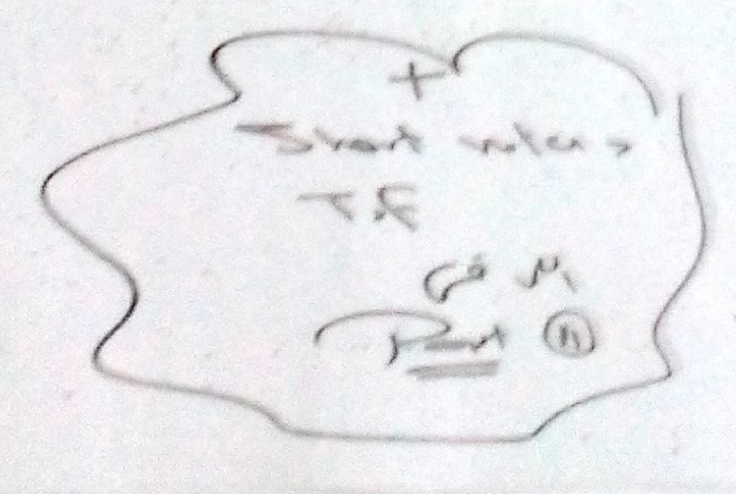
Part XI

**True or False:**

1. The width of MOS transistor increases, its gate capacitance will decrease. [F]
2. The supply voltage of chip increase, the maximum transistor current will not change. [F]
3. Scale $I_{ds}$, current density will increase in MOS transistor. [T]
4. Transconductance of PMOS transistor is negative. [F]
5. Technology shrinks about 0.7 per generation. [T]
6. Polysilicon gates is being replaced by aluminum 1980. [F]
7. In FPGA : the CLB contains 4 LUTs. [F]
8. NMOS transistors, their substrate contacts are connected to ground. [T]
9. CMOS gates, dissipate static power when output is low. [F]
10. A substrate contact is used to tie the semiconductor substrate to ground. [T]
11. FPGA is low non-recurring (NRE) cost. [T]
12. In CMOS process, the effective gate length is often slightly larger than the drawn gate length. [F]
13. Via is between metal layers and diffusion layer. [F]
14. ASIC, high NRE and low design cost. [T]
15. In scaling, designs have higher yield and increased performance. [T]
16. VTC tell us about how fast device is. [T]

b) True Or False : each statement with T Or F.
- If the length a MOS transistor increases,the current will decrease [ ]
- Virtex-5,one slice contains two LUTs [ ]

c) Explain Top-down design. Define RTL,give an example.





13

$C \propto W \propto L$

$I \propto W \propto \frac{1}{L} \propto V$

**Complete:**

1- If the width of transistor increase, the current will ........ (increase).

2- If the length of transistor increase, the current will ........(decrease).

3- If the supply voltage of chip increase, the maximum transistor current will ....(increase).

4- If the width of transistor increase, its gate capacitance will ....(increase).

5- If the length of transistor increase, its gate capacitance will ......(increase).

6- If the supply voltage of a chip increase, the gate capacitance of each transistor will ...... (no change).

7- Non Recurring Engineering (NRE) costs, give one reason ....

- Low unit cost
- High performance
- High volume applications
- Design cost
- Mask tooling costs

8- The pitch of metal1 is equal to ..... (8λ)

9- The pitch of n metals is equal to .... (n×8λ)

10- Changing beta ratio (NMOS size, NMs) changes ..... ($V_{IH}$, $V_{IL}$)

11- Interconnect parasitic cause ......

- Reduce reliability
- Affect performance and power consumption

12- Classes of parasitic ....

- Capacitive (worst)
- Resistive
- Inductor

13- To maximize NM, ________________ (select logic levels at unity gain point of DC transfer characteristics)

14- Give one reason, CMOS inverter at steady state ......

- $I_{DSn} = |I_{DSp}|$
- Advantages of CMOS as no static power dissipation





<u>Give short answers:</u>

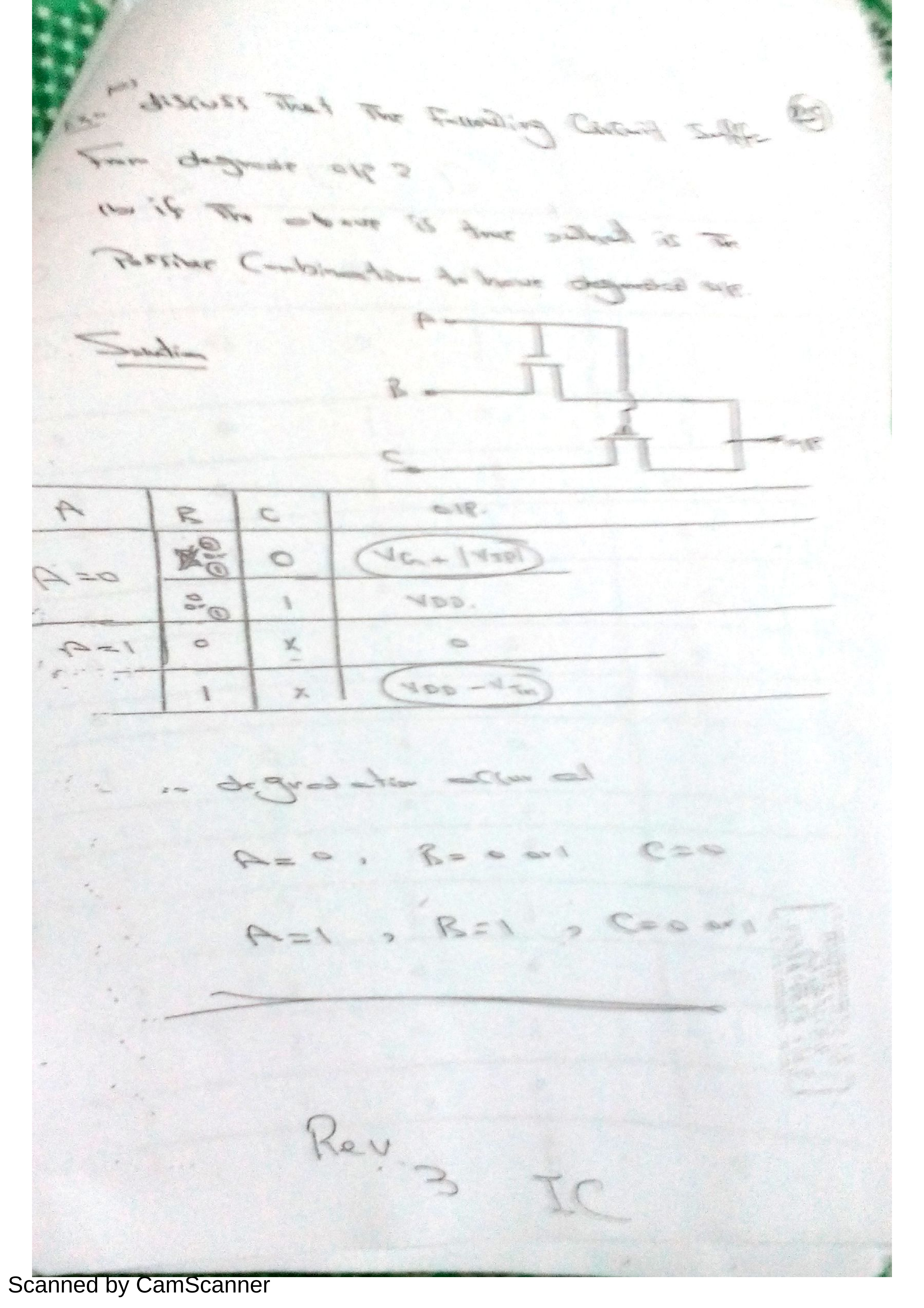
1- Give two reason, advantages of FPGA
   - Good prototype
   - Can be reprogrammed more than one time
2- Static CMOS inverter is not desired on two factors
   - Have two substrate
   - High si area for more than one input
3- Give two reasons, in CMOS gates problem with
   - More si area
   - Complex design
4- Gate speed depends on two factors
   - Parasitic C, R
   - VTC
5- Give two reasons, for difference between ASIC and FPGA
   - FPGA is reprogrammable
   - Short design time
6- Give two reasons, the advantages of digital ICs over discrete components



7- Implementation with single transistor (PTL)
   - Reduce noise margin
   - Causes a static power dissipation
8- Give two reasons, full custom design
   - High performance
   - Used for high volume applications
9- Features of synthesis tools
   - VHDL converted into netlist of basic logic gates
   - Optimization
   - Create EDIF
   - Create bit stream for download

<u>Note:</u>

| Layer | Width | Length |
|---|---|---|
| Poly | 2λ | 3λ |
| Diff | 3λ | 3λ |
| Metal1 | 3λ | 3λ |
| Metal2 | 3λ | 4λ |
| n-well | 10λ | 9λ |
| Cut | 2λ | 2λ |
| via | 2λ | 3λ |



Q3- (m) Discuss that the following circuit suffer from degraded o/p ? (25)

(b) if the above is true what is the possible combination to have degraded o/p.

Solution



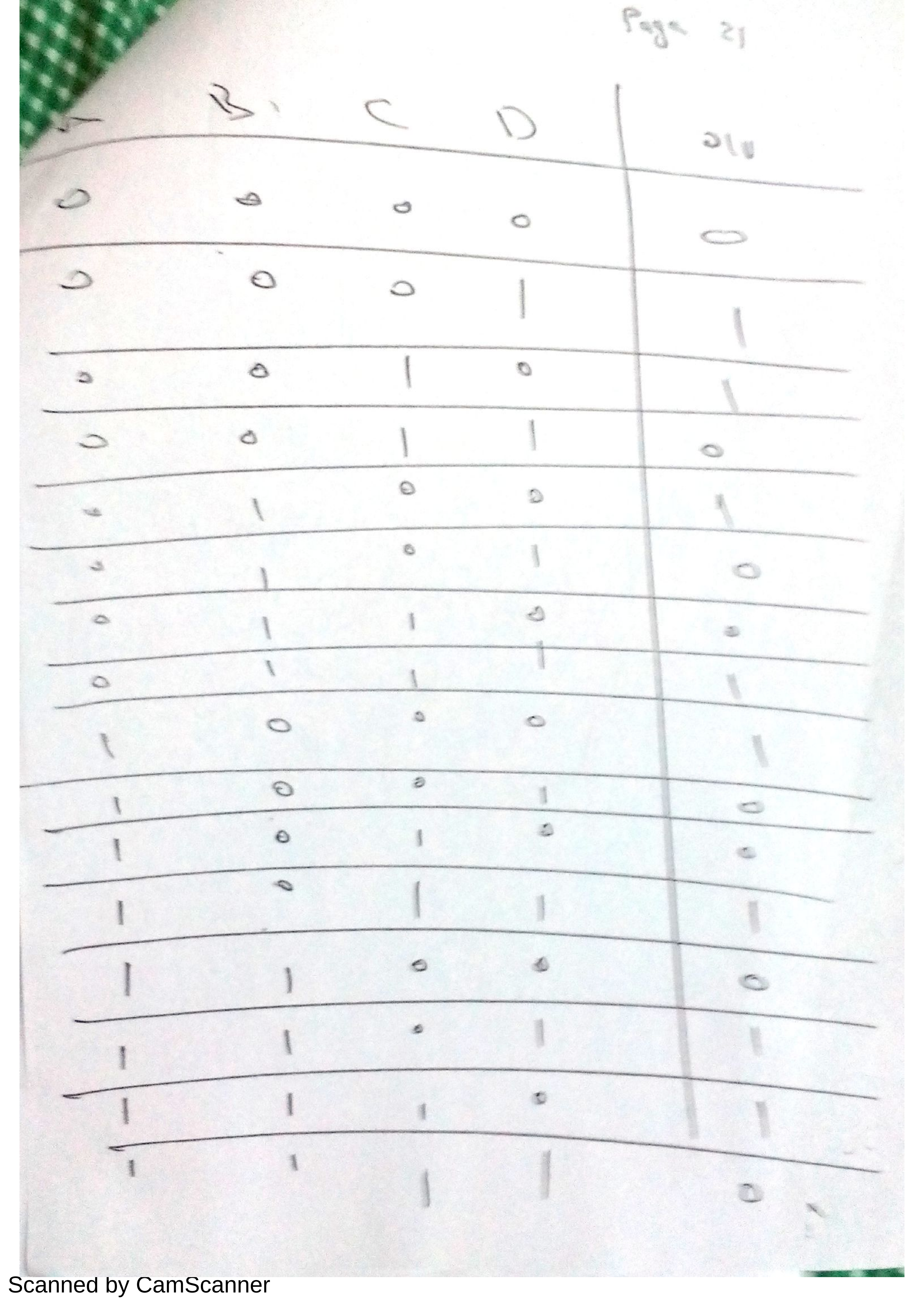
| A | B | C | o/p |
|---|---|---|---|
| A = 0 | 0 or 1 | 0 | $V_{Gn} + \lvert V_{TP} \rvert$ |
| | 0 or 1 | 1 | VDD. |
| A = 1 | 0 | X | 0 |
| | 1 | X | $V_{DD} - V_{tn}$ |

∴ degradation occur at

A = 0 , B = 0 or 1 , C = 0

A = 1 , B = 1 , C = 0 or 1

Rev 3 IC



| A | B | C | D | o/p |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |